AMENDMENTS TO THE DRAWINGS

The attached drawing sheet includes changes to include the claimed integrated circuit.

REMARKS

Claim 6-26 have been examined, with each of these claims rejected based on prior art. More specifically, Claims 6, 19-22, 25, and 26 have been rejected under 35 USC 102(b) as being anticipated by Endroes et al. (U.S. Patent No. 5,650,363; hereinafter "Endroes"). Claims 7, 12-14, and 23 have been rejected under 35 USC 103(a) as being unpatentable over Endroes in view of Bourdelaise et al. (U.S. Patent No. 5,027,191; hereinafter "Bourdelaise"). Claims 15-18 and 24 have been rejected under 35 USC 103(a) as being unpatentable over Endroes in view of Rissing et al. (U.S. Patent Publication No. 2005/0098472; hereinafter "Rissing"). Claims 8-11 have been rejected under 35 USC 103(a) as being unpatentable over Endroes in view of Bourdelaise and Rissing.

Amended independent claim 1 recites "An integrated circuit arrangement comprising a nonplanar substrate in which an integrated circuit is formed on a side of the substrate arranged on a carrier, wherein the carrier is produced from a chemically resistant material." Independent claim 22 recites similar features.

Firstly, the Examiner identifies the non-planar substrate of the integrated circuit arrangement with the protective layer 2 in Figure 3 of Endroes. The description of Endroes shows that the protective layer 2 can be an organic polymer which can act as a photo resist. See column 4, lines 20-25. It can also be a metallically conductive back contact. See column 5, lines 3-6. These layers do not represent a substrate of an integrated circuit arrangement on which an integrated circuit can be placed. Rather, they are deposited on the semiconductor wafer 1, so that the semiconductor wafer 1 of Endroes should be the substrate.

Secondly, the independent claims include an integrated circuit, which the examiner identifies with the solar cell 1 of Endroes. However, while a solar cell can be produced on a semiconductor wafer, it is not an integrated circuit, which usually involves at least one transistor.

Thirdly, Endroes teaches using a glass carrier but fails to disclose that the glass carrier is chemically resistant. There are different grades of glass, and not all grades of glass are chemically resistant.

Also, the integrated circuit is located in a side 3 of the substrate 2 which faces the carrier 4. As a result, it is not possible to analyze or manipulate the integrated circuit. Endroes does not teach that the integrated circuit - if a solar cell can be regarded as such - is placed on the side that is closest to the carrier.

Thus the claims are patentable over the applied references for at least these reasons. Reconsideration and withdrawal of the prior art rejection is therefore respectfully requested.

Finally, the drawings have been objected to as not showing the claimed integrated circuit formed on the one side of the substrate. In response, Applicant submits herewith an amended drawing showing the integrated circuit. Support for this amendment may be found in the published application at paragraph 0015, for example. No new matter has been added. Reconsideration and withdrawal of this objection is respectfully requested.

In view of the above, Applicant believes the pending application is in condition for allowance.

In the event a fee is required or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 50-2215.

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Respectfully submitted,

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